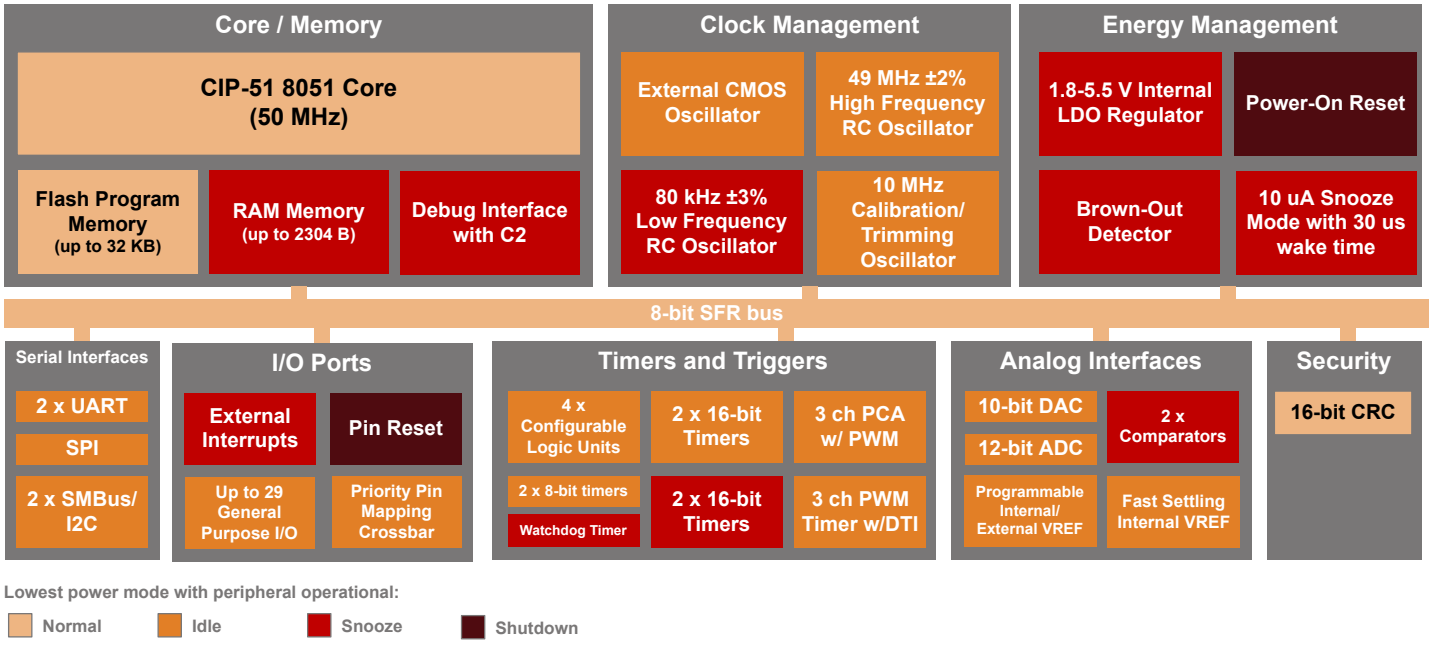
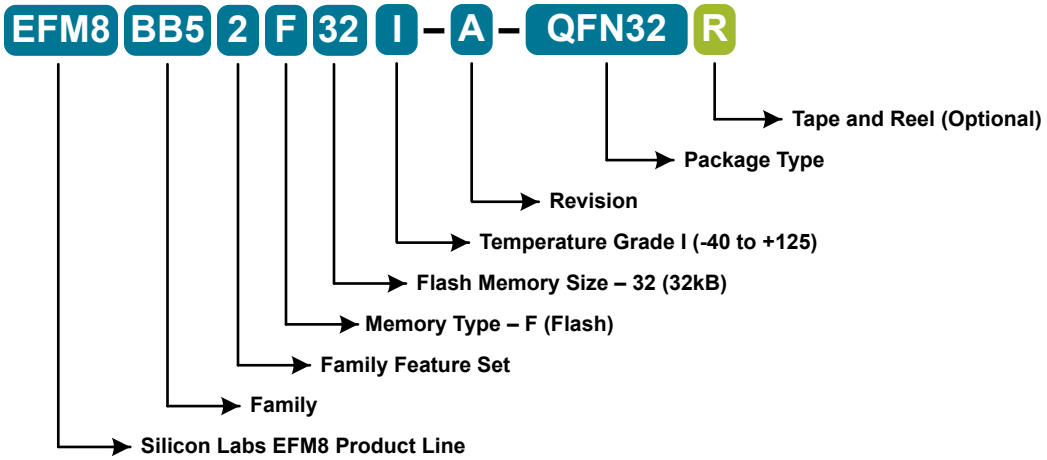
EFM8BB52F32I-C-QFN32 Data Sheet

- Pipelined 8-bit C8051 core with 50 MHz maximum operating frequency (70% of instructions execute in 1-2 clock cycles)
- Up to 29 multifunction, 5 Volt capable I/O pins
- Three Internal Oscillators (49 MHz, 10 MHz, and 80 kHz)
- Snooze power mode with LFO running, 10 µA and 30 µs wake
- 1 x 12-bit 612 ksps Analog-to-Digital Converter (ADC) with 16 channels and 11-bit ENOB
- 1 x 10-bit 200 ksps Digital-to-Analog Converter (DAC)
- 2 x analog comparators with adjustable reference
- Integrated temperature sensor
- 3-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
- 3-channel PWM engine with complementary outputs and dead time insertion (DTI)
- 4 x 16-bit timers
- 2 x 8-bit timers
- 2 x UART up to 3 Mbaud and 2 x SMBus™/I2C™ Leader / Follower up to 400 kbps
- SPI™ with 4 byte FIFO, Main / Secondary up to 12 Mbps
- 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- Priority crossbar for flexible pin mapping
- 4 x configurable logic units
- 1.2 - 2.4 V precision VREF routable to external pin
- Pre-loaded UART bootloader
- 128-bit unique device identifier (UUID)
- Temperature range -40 to 125 ºC
- Single power supply 1.8 to 5.5 V
- QFN32 packages
- Independent watchdog timer, clocked from the low frequency oscillator



Name Information



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1. System Overview

1.1 Introduction

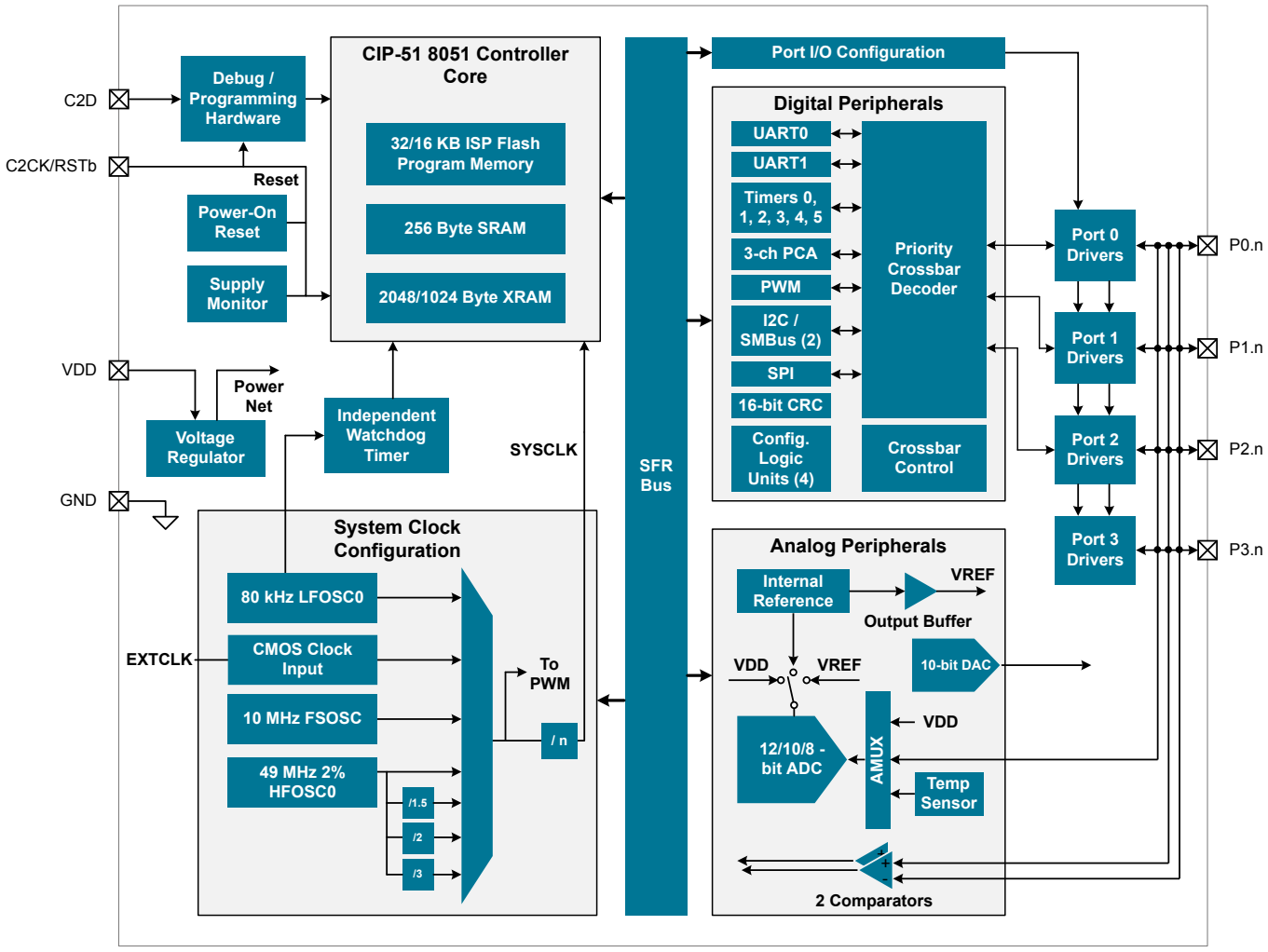

Figure 1.1. Detailed EFM8BB52 Block Diagram

1.2 CIP-51 Microcontroller Core

The CIP-51 microcontroller core is a high-speed, pipelined, 8-bit core utilizing the standard MCS-51™ instruction set. Any standard 803x/805x assemblers and compilers can be used to develop software. The MCU family has a superset of all the peripherals included with a standard 8051. The CIP-51 includes on-chip debug hardware and interfaces directly with the analog and digital subsystems providing a complete data acquisition or control system solution.

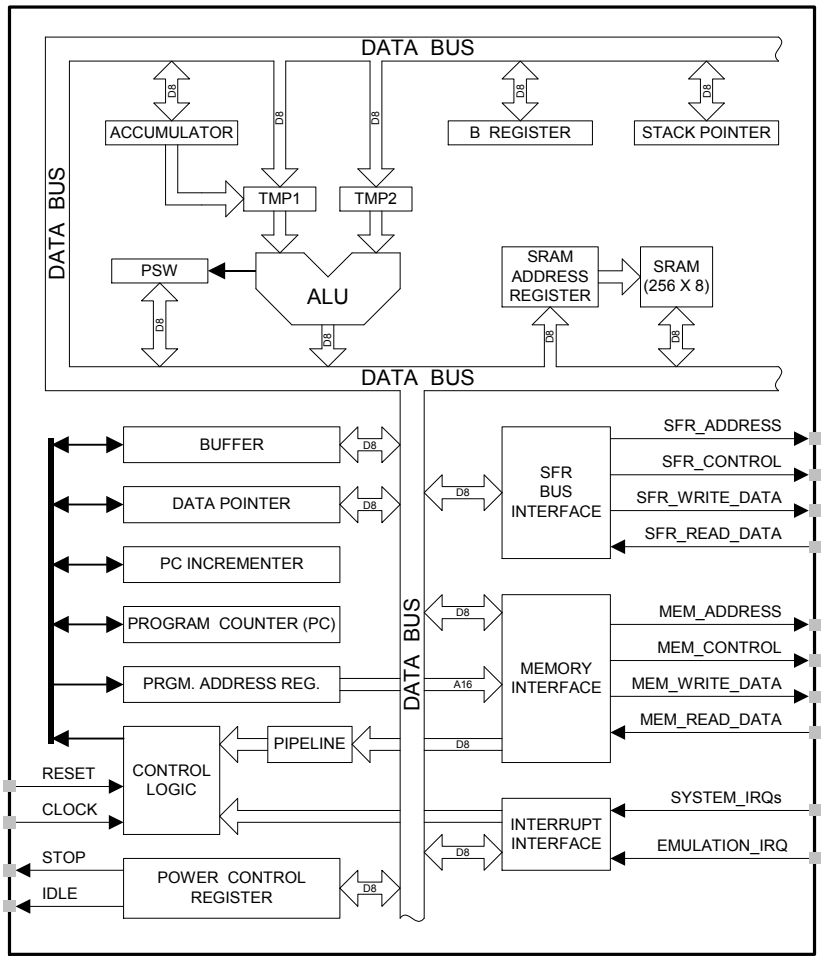

Figure 1.2. CIP-51 Block Diagram

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability. The CIP-51 includes the following features:

- Fast, efficient, pipelined architecture.
- Fully compatible with MCS-51 instruction set.
- 0 to 50 MHz operating clock frequency.
- 50 MIPS peak throughput with 50 MHz clock.
- Extended interrupt handler.
- Power management modes.
- On-chip debug logic.
- Program and data memory security.

1.3 Memory

The memory organization of the CIP-51 System Controller is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. Program memory consists of a non-volatile storage area that may be used for either program code or non-volatile data storage. The data memory, consisting of "internal" and "external" data space, is implemented as RAM, and may be used only for data storage. Program execution is not supported from the data memory space.

Program Memory

The CIP-51 core has a 64 KB program memory space. The product family implements some of this program memory space as in-system, re-programmable flash memory. Flash security is implemented by a user-programmable location in the flash block and provides read, write, and erase protection. All addresses not specified in the device memory map are reserved and may not be used for code or data storage.

Data Memory

The RAM space on the chip includes both an "internal" RAM area which is accessed with MOV instructions, and an on-chip "external" RAM area which is accessed using MOVX instructions. Total RAM varies, based on the specific device. The device memory map has more details about the specific amount of RAM available in each area for the different device variants.

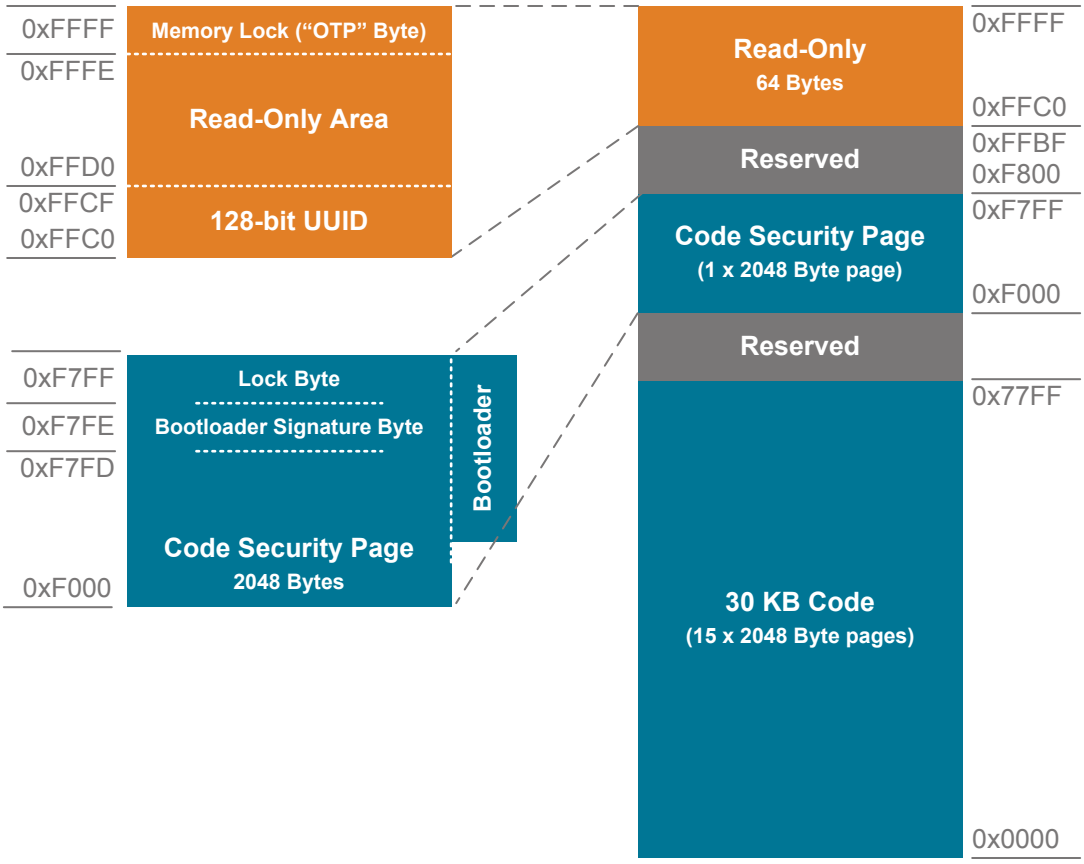

Figure 1.3. Flash Memory Map — 32 KB Devices

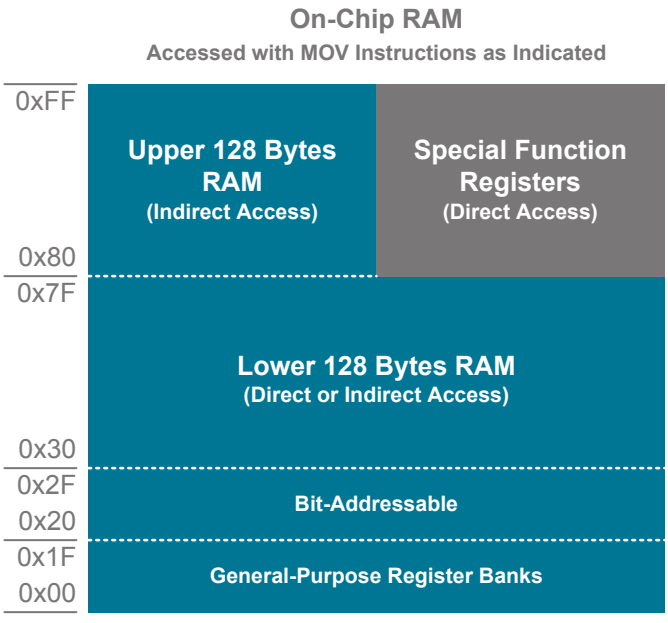

Figure 1.5. Direct / Indirect RAM Memory

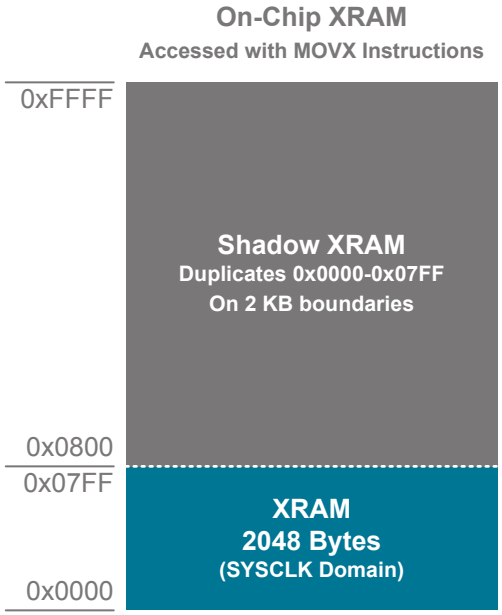

Figure 1.6. XRAM Memory

1.4 Power

All internal circuitry and I/O pins are powered via the VDD supply pin. Most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 1.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Stop	• HFOSC0 oscillator stopped • Pins retain state • Exit on any reset source	1. Clear STOPCF bit in REG0CN 2. Set STOP bit in PCON0	Any reset source
Snooze	• Core and peripheral clocks halted • HFOSC0 and FSOSC0 oscillators stopped • Regulator in low bias current mode for energy savings • Timer 3 and 4 may clock from LFOSC0 • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SNOOZE bit in PCON1	• Timer 4 Event • Port Match Event • Comparator 0 Falling Edge • CLU Interrupt-Enabled Event
Shutdown	• All internal power nets shut down • Pins retain state • Exit on pin or power-on reset	1. Set STOPCF bit in REG0CN 2. Set STOP bit in PCON0	• RSTb pin reset • Power-on reset

1.5 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.7 can be defined as general-purpose I/O (GPIO) or assigned to one of the internal digital resources through the crossbar or dedicated channels. Port pins P0.0-P3.1 can be assigned to an analog function. Port pins P3.0 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.0 or P3.7.

The port control block offers the following features:

- Up to 29 multi-function I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

1.6 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the HFOSC 24.5 MHz output divided by 8 (3.0625 MHz).

The clock control system offers the following features:

- Provides clock to core and peripherals.
- Configurable system clock source:
  - 49 MHz internal oscillator (HFOSC), accurate to ±2% across process, supply, and temperature corners
  - 10 MHz internal oscillator (FSOSC), fast-startup, low power
  - 80 kHz low-frequency oscillator (LFOSC)
  - CMOS external clock input (EXTCLK)
  - 24.5 MHz clock from HFOSC
  - 24.5 MHz clock from HFOSC divided by 1.5 (16.33 MHz)
  - 2.5 MHz clock from FSOSC
  - 49 MHz clock from HFOSC divided by 1.5 (32.67 MHz)
- Clock divider with eight settings for flexible clock scaling:
  - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128

1.7 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware "kill" signal from comparator 0 or comparator 1

Pulse Width Modulation (PWM) Timer

The PWM module provides three channels of enhanced 16-bit Pulse-Width Modulated (PWM) functionality, with complementary outputs and automatic dead-time insertion (DTI).

The PWM module has the following features:

- 16-bit counter, operable up to 50 MHz with programmable overflow
- Time base of pre-divided SYSCLK, allowing full speed operation while core and other peripherals clocked slower
- Up to three single-ended channels
- Up to six differential channels, consisting of the single-ended and their complementary outputs with programmable dead-time
- Four hardware triggers (TIMER2 and TIMER3 overflow, CLU2 and CLU3 asynchronous output) plus software trigger
- Adjustable hardware dead-time insertion, supports positive and negative dead time
- Edge-aligned or center-aligned operation
- External hardware stop signal from Comparator or CLU channel with configurable defined PWM output state

Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture
- LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

1.8 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions
- Dedicated baud rate generator supports baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 5, 6, 7, 8, or 9 bit data
- Automatic start and stop generation
- Automatic parity generation and checking
- Single-byte buffer on transmit and receive
- Auto-baud detection
- LIN break and sync field detection
- CTS / RTS hardware flow control

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a main (clock driver) or secondary (clock receiver) interface in both 3-wire or 4-wire modes, and supports multiple main/secondary devices on a single SPI bus. The chip-select (NSS) signal can be configured as an input to select the SPI in secondary mode, or to disable main mode operation in an environment with multiple main interfaces, avoiding contention on the SPI bus when more than one main device attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in main inferface mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple secondary devices.

- Supports 3- or 4-wire main or secondary interface modes
- Supports external clock frequencies up to 12 Mbps in either mode
- Support for all clock phase and polarity modes
- 8-bit programmable clock rate (main)
- Programmable receive timeout (secondary)
- Four byte FIFO on transmit and receive
- Support for multiple main interfaces on the same data lines

System Management Bus / I2C (SMB0 and SMB1)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- Support for leader, follower, and multi-leader modes
- Hardware synchronization and arbitration for multi-leader mode
- Clock low extending (clock stretching) to interface with faster leader devices
- Hardware support for 7-bit follower and general call address recognition
- Firmware support for 10-bit follower address decoding
- Ability to inhibit all follower states
- Programmable data setup/hold times
- Transmit and receive FIFOs (one byte) to help increase throughput in faster applications

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- Units may be operated synchronously or asynchronously
- May be cascaded together to perform more complicated logic functions
- Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- Can be used to synchronize and trigger multiple on-chip resources (ADC, Timers, etc.)
- Asynchronous output may be used to wake from low-power states

1.9 Analog

12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-bit resolution, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 16 external inputs
- Single-ended 12-bit, 10-bit and 8-bit modes
- Support for an output update rate of up to 612.5 ksps in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers(Only available if ADCCLK is SYSCLK)
- Asynchronous hardware conversion trigger, selectable between software, internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Support for conversion complete and window compare interrupts
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.2 - 1.8 V adjustable reference, with support for using the supply as the reference, an external reference, or an on-chip precision 1.2 - 2.4V reference
- Integrated temperature sensor

10-Bit Digital-to-Analog Converter (DAC0)

The DAC module is a 10-bit Digital-to-Analog Converter. The DAC is fully configurable under software control. The voltage reference for the DAC is selectable between internal and external reference sources.

The DAC includes the following features:

- Voltage output with 10-bit performance
- Supports references from internal supply, on-chip precision reference, or external VREF pin
- Supports an update rate of 200 ksps
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output may be configured to persist through reset and maintain output state to avoid system disruption
- Flexible input data formatting
- Output may be autonomously switched between two levels according to state of configurable logic / PWM input trigger

Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 8 (CMP0) or 11 (CMP1) external positive inputs
- Up to 3 (CMP0) or 3 (CMP1) external negative inputs
- Additional input options:
  - Dedicated 4-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature
- Wakeup source from snooze mode

1.10 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. A reset state will be asserted due to low supply voltage, a low state on the external reset pin, or other configurable reset sources. On entry to this reset state, the core halts all execution and sets registers and external pin ports to known initial values. On exit from the reset state, the program counter (PC) is reset and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

1.11 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

Silicon Labs recommends the bootloader be disabled and the flash memory locked after the production programming step in applications where code security is a concern. More information about the factory bootloader protocol, usage, customization and best practices can be found in *AN945: EFM8 Factory Bootloader User Guide*.

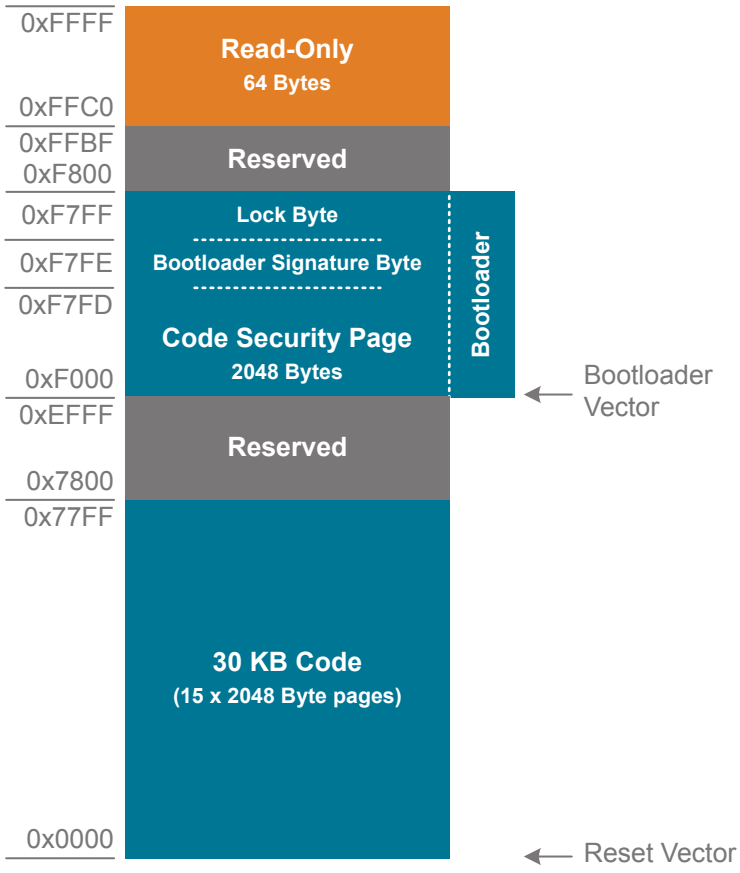

Figure 1.7. Flash Memory Map with Bootloader —32 KB Devices

Table 1.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

Table 1.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QFN32	P3.7 / C2D

2. Electrical Specifications

2.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and all supplies at 3.0 V, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

2.1.1 Absolute Maximum Ratings

Stresses above those listed in Table 4.1 Absolute Maximum Ratings on page 21 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 2.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature	T_{STG}		-50	—	150	°C
Voltage on VDD supply pin	V_{VDDMAX}		GND - 0.3	—	5.5	V
Voltage on GPIO pins	V_{DIGPIN}		GND - 0.3	—	VDD + 0.3	V
Junction temperature	T_{JMAX}	-G grade	—	—	105	°C
		-I grade	—	—	125	°C
Total current into supply pins	I_{VDDMAX}	Source	—	—	200	mA
Total current into ground pins	I_{GNDMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Source	—	—	50	mA
		Sink	—	—	50	mA
Current for all I/O pin	$I_{IOALLMAX}$	Source	—	—	200	mA
		Sink	—	—	200	mA

2.1.2 General Operating Conditions

Table 2.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage on VDD supply pin	V_{VDD}		1.8	—	5.5	V
System clock frequency	f_{SYSCLK}		—	—	50	MHz
Operating ambient temperature	T_A	-G grade	-40	—	85	°C
		-I grade	-40	—	125	°C

2.1.3 Supply Current Consumption at 5 V, 25 °C

All typical and maximum values specified at 25 °C.

Table 2.3. Supply Current Consumption at 5 V, 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Normal Mode, full code execution	I_{NORMAL}	f_SYSCLK = 49 MHz using HFOSC[1]	—	55.5	60	µA/MHz
		f_SYSCLK = 24.5 MHz using HFOSC[1]	—	81	90	µA/MHz
		f_SYSCLK = 1.53 MHz using HFOSC[1]	—	691	810	µA/MHz
		f_SYSCLK = 80 kHz using LFOSC[2]	—	648	830	µA
Idle Mode, core halted with peripherals running	I_{IDLE}	f_SYSCLK = 49 MHz using HFOSC[1]	—	44	49	µA/MHz
		f_SYSCLK = 24.5 MHz using HFOSC[1]	—	62	70	µA/MHz
		f_SYSCLK = 1.53 MHz using HFOSC[1]	—	673	800	µA/MHz
		f_SYSCLK = 80 kHz using LFOSC[2]	—	648	830	µA
Snooze Mode, core halted and high-frequency clocks stopped, regulator in low-power state	I_{SNOOZE}	LFOSC running at 80 kHz	—	10.9	15.3	µA
		No LFOSC	—	9.8	14.2	µA
Stop Mode, core halted, all clocks stopped, internal reglators on, supply monitor off	I_{STOP}		—	930	1150	µA
Shutdown Mode, core halted, all clocks stopped, internal reglators off, supply monitor off	$I_{SHUTDOWN}$		—	1.3	1.8	µA

Note:

1. Includes current from internal regulators, supply monitor, and HFOSC
2. Includes current from internal regulators, supply monitor, and LFOSC

2.1.4 Maximum Supply Current Consumption at 5 V, 125 °C

All maximum values specified at 125 °C.

Table 4.4. Maximum Supply Current Consumption at 5 V, 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Normal Mode, full code execution	I_{NORMAL}	f_SYSCLK = 49 MHz using HFOSC[1]	—	—	63	µA/MHz
		f_SYSCLK = 24.5 MHz using HFOSC[1]	—	—	95	µA/MHz
		f_SYSCLK = 1.53 MHz using HFOSC[1]	—	—	880	µA/MHz
		f_SYSCLK = 80 kHz using LFOSC[2]	—	—	925	µA
Idle Mode, core halted with peripherals running	I_{IDLE}	f_SYSCLK = 49 MHz using HFOSC[1]	—	—	52	µA/MHz
		f_SYSCLK = 24.5 MHz using HFOSC[1]	—	—	75	µA/MHz
		f_SYSCLK = 1.53 MHz using HFOSC[1]	—	—	875	µA/MHz
		f_SYSCLK = 80 kHz using LFOSC[2]	—	—	925	µA
Snooze Mode, core halted and high-frequency clocks stopped, regulator in low-power state	I_{SNOOZE}	LFOSC running at 80 kHz	—	—	170	µA
		No LFOSC	—	—	170	µA
Stop Mode, core halted, all clocks stopped, internal reglators on, supply monitor off	I_{STOP}		—	—	1250	µA
Shutdown Mode, core halted, all clocks stopped, internal reglators off, supply monitor off	$I_{SHUTDOWN}$		—	—	30	µA

Note:

1. Includes current from internal regulators, supply monitor, and HFOSC
2. Includes current from internal regulators, supply monitor, and LFOSC

2.1.5 Typical Supply Current Consumption at 3.3 V, 25 °C

All typical values specified at 25 °C.

Table 2.5. Typical Supply Current Consumption at 3.3 V, 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Normal Mode, full code execution	I_{NORMAL}	f_SYSCLK = 49 MHz using HFOSC[1]	—	57	—	µA/MHz
		f_SYSCLK = 24.5 MHz using HFOSC[1]	—	82	—	µA/MHz
		f_SYSCLK = 1.53 MHz using HFOSC[1]	—	690	—	µA/MHz
		f_SYSCLK = 80 kHz using LFOSC[2]	—	645	—	µA
Idle Mode, core halted with peripherals running	I_{IDLE}	f_SYSCLK = 49 MHz using HFOSC[1]	—	45	—	µA/MHz
		f_SYSCLK = 24.5 MHz using HFOSC[1]	—	63	—	µA/MHz
		f_SYSCLK = 1.53 MHz using HFOSC[1]	—	673	—	µA/MHz
		f_SYSCLK = 80 kHz using LFOSC[2]	—	645	—	µA
Snooze Mode, core halted and high-frequency clocks stopped, regulator in low-power state	I_{SNOOZE}	LFOSC running at 80 kHz	—	9.3	—	µA
		No LFOSC	—	8.3	—	µA
Stop Mode, core halted, all clocks stopped, internal reglators on, supply monitor off	I_{STOP}		—	924	—	µA
Shutdown Mode, core halted, all clocks stopped, internal reglators off, supply monitor off	$I_{SHUTDOWN}$		—	0.24	—	µA

Note:

1. Includes current from internal regulators, supply monitor, and HFOSC
2. Includes current from internal regulators, supply monitor, and LFOSC

2.1.6 Typical Supply Current Consumption at 1.8 V, 25 °C

All typical values specified at 25 °C.

Table 2.6. Typical Supply Current Consumption at 1.8 V, 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Normal Mode, full code execution	I_{NORMAL}	f_SYSCLK = 49 MHz using HFOSC[1]	—	56	—	µA/MHz
		f_SYSCLK = 24.5 MHz using HFOSC[1]	—	81	—	µA/MHz
		f_SYSCLK = 1.53 MHz using HFOSC[1]	—	669	—	µA/MHz
		f_SYSCLK = 80 kHz using LFOSC[2]	—	612	—	µA
Idle Mode, core halted with peripherals running	I_{IDLE}	f_SYSCLK = 49 MHz using HFOSC[1]	—	45	—	µA/MHz
		f_SYSCLK = 24.5 MHz using HFOSC[1]	—	62	—	µA/MHz
		f_SYSCLK = 1.53 MHz using HFOSC[1]	—	504	—	µA/MHz
		f_SYSCLK = 80 kHz using LFOSC[2]	—	612	—	µA
Snooze Mode, core halted and high-frequency clocks stopped, regulator in low-power state	I_{SNOOZE}	LFOSC running at 80 kHz	—	10.0	—	µA
		No LFOSC	—	9.0	—	µA
Stop Mode, core halted, all clocks stopped, internal reglators on, supply monitor off	I_{STOP}		—	890	—	µA
Shutdown Mode, core halted, all clocks stopped, internal reglators off, supply monitor off	$I_{SHUTDOWN}$		—	0.19	—	µA

Note:

1. Includes current from internal regulators, supply monitor, and HFOSC
2. Includes current from internal regulators, supply monitor, and LFOSC

2.1.7 Reset and Supply Monitor

Table 2.7. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD supply monitor threshold [1]	V_{VDDM}	Falling voltage on V_{VDD}	1.67	1.71	1.75	V
Power-on reset (POR) threshold	V_{POR}	Rising voltage on V_{VDD}	—	1.76	1.8	V
Supply ramp rate[1]	$RAMP_{VDD}$		10	—	—	us/V
Reset delay from POR	t_{POR}	Relative to $V_{VDD} > V_{POR}$, ramp to V_{POR} in ≤ 100 µs	—	220	390	µs
Reset delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	100	200	µs
Missing clock detector response time	t_{MCD}	Time between final rising edge and reset, $F_{SYSCLK} > 1$ MHz	—	0.25	0.38	ms
Missing clock detector trigger frequency	f_{MCD}		—	6.5	10	kHz
RSTb low time to generate reset[2]	t_{RSTL}		15	—	—	µs

Note:

1. V_{VDDM} is a parameter that is calibrated and adjusted shortly after reset. The circuit uses the initial, uncalibrated value directly out of any reset. On some devices, the uncalibrated V_{VDDM} level may be lower than the calibrated V_{VDDM} value, resulting in multiple reset pulses on the RST pin if the supply voltage remains between these two levels.
2. If the device is in Snooze mode when a pin reset occurs, the reset sequence will be initiated by the minimum time specified, but the device may require up to 130 µs to fully complete this reset.

2.1.8 Wakeup Timing

Table 2.8. Wakeup Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Idle mode wake-up time	t_{IDLEWK}	Entered Idle mode running from HFOSC	2	—	3	SYSCLKs
		Entered Idle mode running from LFOSC	4	—	5	SYSCLKs
Snooze mode wake-up time	$t_{SNOOZEWK}$	SYSCLK = HFOSC, CLKDIV = 0x00, System in Snooze when wake event occurs.	—	30	50	µs

2.1.9 Flash Memory Characteristics

Table 2.9. Flash Memory Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_VDD voltage during programming[1]	V_{PROG}		2.3	—	5.5	V
Flash supply monitor threshold[1]	V_{FMON}		2.3	—	—	V
Write time[2]	t_{WRITE}	One byte, F_{SYSCLK} = 24.5 MHz	66.5	70	73.5	µs
Erase time[2]	t_{ERASE}	One page, F_{SYSCLK} = 24.5 MHz	24.7	26	27.3	µs
Flash erase cycles before failure[3]	EC_{FLASH}	T_A ≤ 125 °C	10k	—	—	cycles
Flash data retention	RET_{FLASH}	T_A ≤ 125 °C	10	—	—	years
CRC calculation time	t_{CRC}	Per 256-byte block, SYSCLK = 49 MHz	—	5.4	—	µs

Note:
1. The flash supply monitor prevents flash programming operations below the minimum safe supply voltage.
2. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
3. Flash data retention information is published in the Quarterly Quality and Reliability Report.

2.1.10 High-Frequency Oscillator

Table 2.10. High-Frequency Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HFOSC oscillator frequency	f_{HFOSC}		48	49	50	MHz
Power supply sensitivity	PSS_{HFOSC}	T_A = 25 °C	—	0.026	—	%/V
Temperature sensitivity	TS_{HFOSC}	V_{VDD} = 3.0 V	—	140	—	ppm/°C
HFOSC start-up time	$t_{STARTUP}$		—	3.75	—	µs

2.1.11 Low-Frequency Oscillator

Table 2.11. Low-Frequency Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LFOSC oscillator frequency	f_{LFOSC}		77.6	80	82.4	kHz
Power supply sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	0.08	—	%/V
Temperature sensitivity	TS_{LFOSC}	V_{VDD} = 3.0 V	—	66	—	ppm/°C
LFOSC start-up time	$t_{STARTUP}$		—	11.1	—	µs

2.1.12 Fast-Start Oscillator

Table 2.12. Fast-Start Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSOSC oscillator frequency	f_{FSOSC}		9	10	11	MHz
power supply sensitivity	PSS_{FSOSC}	T_A = 25 °C	—	0.1	—	%/V
Temperature sensitivity	TS_{FSOSC}	V_{VDD} = 3.0 V	—	2000	—	ppm/°C
FSOSC start-up time	$t_{STARTUP}$		—	0.48	—	µs

2.1.13 External Clock Input

Table 2.13. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External clock frequency	f_{CMOS}	Clock provided at EXTCLK pin	0	—	50	MHz
External clock high time	t_{CMOSH}		9	—	—	ns
External clock low time	t_{CMOSL}		9	—	—	ns

2.1.14 Analog to Digital Converter (ADC)

Table 2.14. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	Resolution	Three resolution settings, 12 bit, 10 bit, and 8 bit	8	—	12	bits
Throughput rate	f_{SAMPLE}	12-bit conversion	—	—	612.5	ksps
		10-bit conversion	—	—	680	ksps
		8-bit conversion	—	—	765	ksps
Conversion time	$t_{CONVERT}$	12-bit conversion	—	30	—	clocks
		10-bit conversion	—	26	—	clocks
		8-bit conversion	—	22	—	clocks
Required tracking time	t_{TRACK}		400	—	—	ns
SAR clock frequency	f_{SAR}		12.5	—	25	MHz
Power-on time	t_{PWR}		—	—	5	µs
Sample/Hold capacitor	C_{SAR}	Gain = 1	—	2	—	pF
		Gain = 0.75	—	1.5	—	pF
		Gain = 0.5	—	1	—	pF
		Gain = 0.25	—	0.5	—	pF
Input mux series impedance	R_{MUX}		—	1.5	—	kΩ
Voltage reference range	V_{REF}	VDD as reference	1.2	—	VDD	V
		External reference via ADC0.VREF	1.2	—	2.5	V
Internal fast-start reference startup time	t_{FSREF}		—	—	5	µs
Internal fast-start reference power supply rejection ratio	$PSRR_{FSREF}$		—	116	—	ppm/V
Internal fast-start reference voltage	V_{FSREF}	REFSL = 0x2 (1.65 V Setting), VDD ≥ 2.2 V	1.61	1.65	1.69	V
		REFSL = 0x1 (1.4 V Setting)	1.36	1.4	1.44	V
		REFSL = 0x0 (1.2 V Setting)	1.17	1.2	1.23	V
		REFSL = 0x3 (1.8 V Setting), VDD ≥ 2.2 V	1.75	1.8	1.85	V
Internal fast-start reference temperature coefficient	TC_{FSREF}		—	66	—	ppm/°C
External voltage reference input current	$I_{EXTVREF}$	Sample rate = 612.5 ksps	—	5	—	µA
Voltage on VDD when used as VREF	V_{VDDREF}	REFSL = 0x4 (VDD * 24/68)	3.4	—	5.5	V
		REFSL = 0x5 (VDD * 34/68)	2.3	—	3.7	V
		REFSL = 0x6 (VDD * 46/68)	1.8	—	2.9	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current for VDD divider when VDD used as VREF	I_{VDDREF}	REFSL = 0x4, 0x5, or 0x6	—	16	—	µA
Input measurement range	V_{IN}		—	—	VREF / Gain	V
Maximum voltage at pin	V_{IN_MAX}		—	—	VDD	V
ADC supply current[1]	I_{ADC}	Full speed, 612.5 ksps, 12-bit conversions	—	250	315	µA
Internal fast-start reference supply current	I_{FSREF}	1.2 V Setting	—	86	103	µA
Integral nonlinearity	INL	12-bit conversion	-2.6	—	1.9	LSB
Differential nonlinearity	DNL	12-bit conversion	-1	—	1.6	LSB
Offset error[2]	E_{OFFSET}	12-bit conversion	-3.5	—	2.1	LSB
Full-scale error	E_{FS}	12-bit conversion	-3.5	—	2.3	LSB
Effective number of bits	ENOB	Gain = 1, 12-bit conversion[3]	10.8	—	—	bits
Signal-to-Noise	SNR	Gain = 1, 12-bit conversion[3]	67	72	—	dB
Signal-to-Noise Plus Distortion	SNDR	Gain = 1, 12-bit conversion[3]	64	71	—	dB
Total Harmonic Distortion	THD	Gain = 1, 12-bit conversion[3]	—	-74	-64	dB
Spurious-Free Dynamic Range	SFDR	Gain = 1, 12-bit conversion[3]	65	76	—	dB
Power supply rejection ratio	PSRR	At 1 kHz	—	73	—	dB

Note:

1. Does not include current from analog mux charge-pump.
2. Offset is specified using curve fitting and measured using a linear search where the intercept is always positive.
3. Input is 10 kHz sine wave, 1 dB below full scale. ADC using external VREF and AGND pin and sampling at full speed.

2.1.15 Temperature Sensor

Table 2.15. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Start-up time	t_{TSENSE}		—	4	6	µs
Offset voltage	V_{OFF_TSENSE}	T_A = 0 °C	—	883	—	mV
Offset error[1]	E_{OFF_TSENSE}	T_A = 0 °C	—	20	—	mV
Nominal slope	M_{TSENSE}		—	2.95	—	mV/°C
Slope error[1]	E_{M_TSENSE}		-200	—	200	µV/°C
Supply current	I_{TSENSE}		—	50	60	µA
Linearity	LIN_{TSENSE}		—	1.5	—	°C
Total error[2]	E_{TOT_TSENSE}		-7.5	—	7.5	°C

Note:

1. Represents one standard deviation from the mean.
2. The temp sensor error includes the offset error, slope error, and linearity error. The values are based upon characterization and are not tested across temperature in production. The values represent three standard deviations above and below the mean.

2.1.16 Precision Voltage Reference (VREF)

Table 2.16. Precision Voltage Reference (VREF)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage at VREF pin	V_{VREFP}	1.2 V setting, full temperature range, V_{VDD} ≥ 1.8 V	1.18	1.2	1.22	V
		1.65 V setting, full temperature range, V_{VDD} ≥ 1.95 V	1.62	1.65	1.67	V
		1.8 V setting, full temperature range, V_{VDD} ≥ 2.1 V	1.77	1.8	1.83	V
		2.4 V setting, full temperature range, V_{VDD} ≥ 2.7 V	2.36	2.4	2.43	V
Turn-on time	t_{VREFP}	0.1 µF bypass on VREF pin, Settling to 8 LSB12	—	110	—	µs
Temperature coefficient	TC_{VREFP}		—	75	—	ppm/°C
Load regulation	LR_{VREFP}	2.4 V setting, Load = 0 to 1 mA, sourced	—	4.5	—	µV/µA
Bypass capacitor	C_{VREFP}		0.1	—	—	µF
Supply current	I_{VREFP}	Does not include load	—	55	67	µA
Short-circuit current	ISC_{VREFP}		—	—	14.1	mA
Power supply rejection ratio	$PSRR_{VREFP}$		—	64	—	dB

4.1.17 Digital to Analog Converter (DAC)

Table 4.17. Digital to Analog Converter (DAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage	V_{OUT}	Gain = 1 (GAINADJ = 0)	0	—	VREF	V
		Gain = 2 (GAINADJ = 1)	0	—	MIN(2*VREF, VDD)	V
Voltage reference range	V_{REF}		1	—	VDD	V
Output current	I_{OUT}		-2	—	2	mA
Resolution	Resolution		—	10	—	bits
Throughput rate	f_{SAMPLE}		—	—	200	ksps
Integral nonlinearity	INL		-1.1	+/-0.4	1.4	LSB
Differential nonlinearity	DNL		-1.4	+/-0.25	0.8	LSB
Slew rate	SR		—	1.4	—	V/µs
Settling time	t_{SETTLE}	25% to 75% full scale step, settling to 10 LSB	—	1.6	5	µs
Power-on time	t_{PWR}	Enable to 90% full scale output, settling to 10 LSB	—	3.3	7.3	µs
Total harmonic distortion	THD	V_{OUT} = 10 kHz sine wave, 10% to 90% full scale	—	-67.5	—	dB
Power supply rejection ratio	PSRR	DC output, V_{OUT} = 50% full scale	—	90	—	dB
Offset error	E_{OFFSET}	VREF = 2.4 V	-4	+/-1	7	LSB
Full scale error	E_{FS}	VREF = 2.4 V	-4.1	+/-1	8	LSB
External load impedance	R_L		5	—	—	kΩ
External load capacitance	C_L		—	—	50	pF
Load regulation	LR	V_{OUT} = 50% full scale, I_{OUT} = -2 to 2 mA	—	390	800	µV/mA
DAC supply current[1]	I_{DAC}	Full speed (200 ksps)	—	55	85	µA

Note:

1. Does not include current from analog mux charge-pump.

2.1.18 Analog Comparators (CMP)

Table 2.18. Analog Comparators (CMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input pin voltage	V_{IN}		0	—	VDD	V
Response time	t_{RESP}	CPMD = 0 (highest speed and power), 100 mV differential	—	171	—	ns
		CPMD = 3 (lowest speed and power), 100 mV differential	—	1.82	—	µs
Positive Hysteresis	HYS_{POS}	CPHYP = 0	—	0	—	mV
		CPHYP = 1	—	12	—	mV
		CPHYP = 2	—	24	—	mV
		CPHYP = 3	—	51	—	mV
Negative Hysteresis	HYS_{NEG}	CPHYN = 0	—	0	—	mV
		CPHYN = 1	—	12	—	mV
		CPHYN = 2	—	24	—	mV
		CPHYN = 3	—	51	—	mV
Input pin capacitance	C_{IN}		—	2.8	—	pF
Input offset voltage	V_{OFF}	CPMD = 0, 25 °C	-10	1.7	10	mV
Input offset temperature coefficient	TC_{OFF}		—	0.026	—	mV/°C
Common mode rejection ratio	CMRR		—	69	—	dB
Power supply rejection ratio	PSRR		—	83	—	dB
Compatator supply current[1]	I_{CMP}	CPMD = 0	—	7.4	—	µA
		CPMD = 1	—	3.9	—	µA
		CPMD = 2	—	2.3	—	µA
		CPMD = 3	—	0.5	—	µA
Internal comparator reference DAC resolution	N_{CMPREF}		—	—	4	bits
Comparator reference impedance[2]	R_{CMPREF}		—	960	—	kΩ

Note:

1. Does not include current from analog mux charge-pump.
2. The comparator reference impedance is the total resistance of the reference DAC ladder between VDD and GND. Supply current increase when the reference is used is equal to the supply voltage divided by this resistance.

2.1.19 General Purpose I/O

Table 2.19. General Purpose I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output high voltage	V_{OH}	High drive, I_{OH} = -10 mA, VDD ≥ 3.0 V	VDD - 0.6	—	—	V
		High drive, I_{OH} = -9 mA, 2.2 ≤ VDD < 3.0 V	0.8 * VDD	—	—	V
		High drive, I_{OH} = -6 mA, VDD < 2.2 V	0.8 * VDD	—	—	V
		Low drive, I_{OH} = -3 mA, VDD ≥ 3.0 V	VDD - 0.6	—	—	V
		Low drive, I_{OH} = -2.5 mA, 2.2 ≤ VDD < 3.0 V	0.8 * VDD	—	—	V
		Low drive, I_{OH} = -2 mA, VDD < 2.2 V	0.8 * VDD	—	—	V
Output low voltage	V_{OL}	High drive, I_{OL} = 10 mA, VDD ≥ 3.0 V	—	—	0.6	V
		High drive, I_{OL} = 8 mA, 2.2 ≤ VDD < 3.0 V	—	—	0.2 * VDD	V
		High drive, I_{OL} = 5 mA, VDD < 2.2 V	—	—	0.2 * VDD	V
		Low drive, I_{OL} = 3 mA, VDD ≥ 3.0 V	—	—	0.6	V
		Low drive, I_{OL} = 2.5 mA, 2.2 ≤ VDD < 3.0 V	—	—	0.2 * VDD	V
		Low drive, I_{OL} = 2 mA, VDD < 2.2 V	—	—	0.2 * VDD	V
Input high voltage	V_{IH}		0.7 * VDD	—	—	V
Input low voltage	V_{IL}		—	—	0.3 * VDD	V
Pin capacitance	C_{IO}		—	2	—	pF
Pull-up resistance	R_{PU}		70	130	220	kΩ
Input leakage (pull-up disabled or analog mode)	I_{LK}		—	0.01	2	µA

2.1.20 Configurable Logic

Table 2.20. Configurable Logic

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation delay	t_{DLY}	Single CLU, external pin connections	—	—	53	ns
		Single CLU, internal connections	—	3.6	6.3	ns
Clocking frequency	f_{CLK}	1, 2, or 3 CLUs cascaded	—	—	50	MHz
		4 CLUs cascaded	—	—	45	MHz

2.1.21 SMBus Timing

Table 2.21. SMBus Leader Timing Standard Mode (100 kHz class)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I2C operating frequency[1]	f_{I2C}		0	—	70	kHz
SMBus operating frequency[2, 1]	f_{SMB}		40	—	70	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time[3]	t_{HIGH}		9.4	—	50	µs
SDA set-up time[4]	t_{SU_DAT}		300	—	—	ns
SDA hold time[4]	t_{HD_DAT}		275	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		9.4	—	—	µs
Repeated START condition hold time	t_{HD_STA}		4.7	—	—	µs
STOP condition set-up time	t_{SU_STO}		9.4	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		9.4	—	—	µs
Detect clock low timeout	$t_{TIMEOUT}$		25	—	—	ms

Note:

1. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.
2. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
3. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.
4. Data setup and hold timing at 40 MHz or lower with EXTHOLD set to 1. The DLYEXT bit can be used to adjust the data setup and hold times.

Table 2.22. SMBus Leader Timing Fast Mode (400 kHz class)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I2C operating frequency[1]	f_{I2C}		0	—	256	kHz
SMBus operating frequency[2, 1]	f_{SMB}		40	—	256	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time[3]	t_{HIGH}		2.6	—	50	µs
SDA set-up time[4]	t_{SU_DAT}		300	—	—	ns
SDA hold time[4]	t_{HD_DAT}		275	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		2.6	—	—	µs
Repeated START condition hold time	t_{HD_STA}		1.3	—	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STOP condition set-up time	t_{SU_STO}		2.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		2.6	—	—	µs
Detect clock low timeout	$t_{TIMEOUT}$		25	—	—	ms

Note:

1. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.
2. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
3. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.
4. Data setup and hold timing at 40 MHz or lower with EXTHOLD set to 1. The DLYEXT bit can be used to adjust the data setup and hold times.

Table 2.23. SMBus Peripheral Timing Generation Formulas

Parameter	Symbol	Clocks
SMBus / I2C operating frequency	f_{SMB} f_{I2C}	f_{CSO} / 3
Bus free time between a STOP and START condition	t_{BUF}	2 / f_{CSO}
Repeated START condition hold time	t_{HD_STA}	1 / f_{CSO}
Repeated START condition set-up time	t_{SU_STA}	2 / f_{CSO}
STOP condition set-up time	t_{SU_STO}	2 / f_{CSO}
SCL clock low time	t_{LOW}	1 / f_{CSO}
SCL clock high time	t_{HIGH}	2 / f_{CSO}

Note:

1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

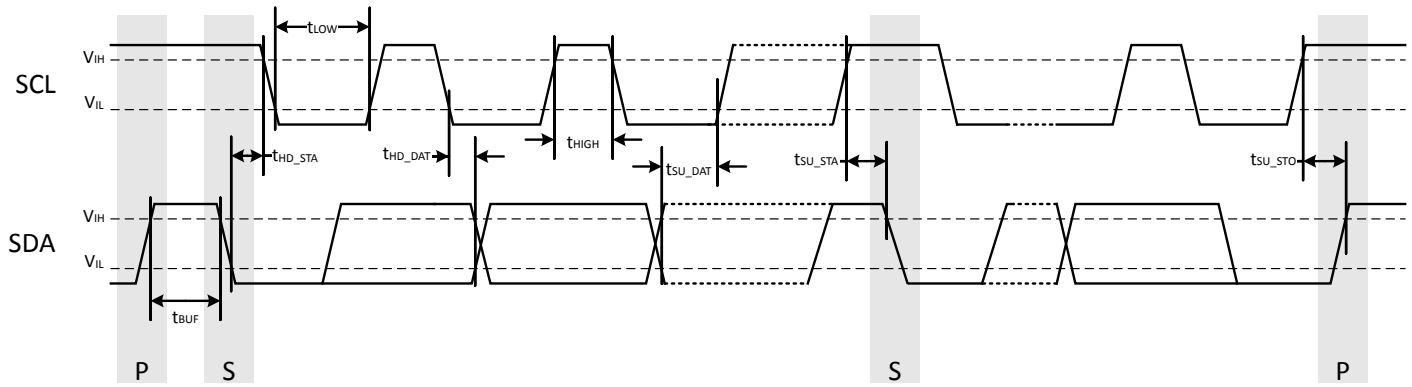

Figure 2.1. SMBus Peripheral Timing Diagram

2.1.22 SPI Timing

Table 2.24. SPI Main Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}	SCLK is derived from SYSCLK, with the fastest possible option being 2 * t_{SYSCLK}. The generated SCLK period should not be faster than the specified minimum.	80	—	—	ns
SCLK to MOSI [1] [2]	t_{SCLK_MO}		-2.5	—	4.5	ns
MISO setup time [1] [2]	t_{SU_MI}		6	—	—	ns
MISO hold time [1] [2]	t_{H_MI}		20	—	—	ns

Note:

1. Applies for both CKPHA = 0 and CKPHA = 1
2. Measurement performed with 5-10 pF loading on output pins at 10% and 90% of V_{VDD}. Assumed transition timing on input pins is 5.5 ns.
3. t_{SYSCLK} is one period of the selected SYSCLK.

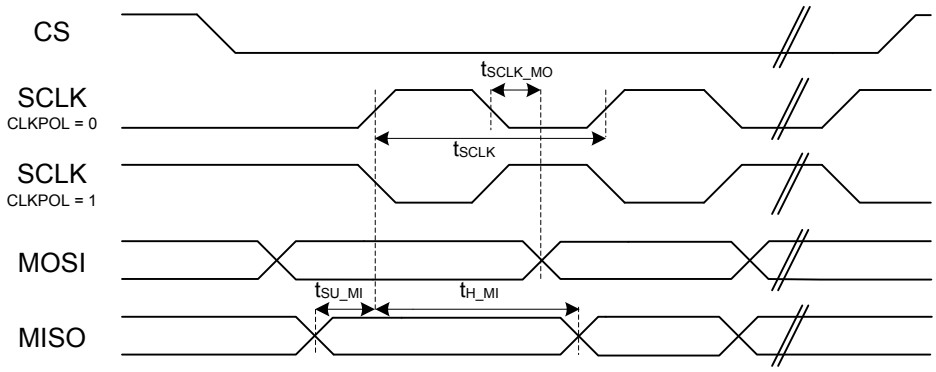

Figure 2.2. SPI Main Timing

Table 2.25. SPI Secondary Timing with 3.0 to 5.5 V supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		80	—	—	ns
SCLK high time [1] [2] [3]	t_{SCLK_HI}		40	—	—	ns
SCLK low time [1] [2] [3]	t_{SCLK_LO}		40	—	—	ns
CS active to MISO [1] [2]	$t_{CS\_ACT\_MI}$		24	—	28	ns
CS disable to MISO [1] [2]	$t_{CS\_DIS\_MI}$		14	—	18	ns
MOSI setup time [1] [2]	t_{SU_MO}		12	—	—	ns
MOSI hold time [1] [2] [3]	t_{H_MO}		10	—	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK to MISO [1] [2] [3]	t_{SCLK_MI}		17	—	34	ns

Note:

1. Applies for both CKPHA = 0 and CKPHA = 1.
2. Measurement performed with 5-10 pF loading on output pins at 10% and 90% of V_{VDD}. Assumed transition timing on input pins is 5.5 ns.
3. t_{SYSCLK} is one period of the selected SYSCLK.

Table 2.26. SPI Secondary Timing with 1.8 to 3.0 V supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		120	—	—	ns
SCLK high time [1] [2] [3]	t_{SCLK_HI}		60	—	—	ns
SCLK low time [1] [2] [3]	t_{SCLK_LO}		60	—	—	ns
CS active to MISO [1] [2]	$t_{CS\_ACT\_MI}$		37	—	41	ns
CS disable to MISO [1] [2]	$t_{CS\_DIS\_MI}$		18	—	21	ns
MOSI setup time [1] [2]	t_{SU_MO}		16	—	—	ns
MOSI hold time [1] [2] [3]	t_{H_MO}		13	—	—	ns
SCLK to MISO [1] [2] [3]	t_{SCLK_MI}		20	—	55	ns

Note:

1. Applies for both CKPHA = 0 and CKPHA = 1.
2. Measurement performed with 5-10 pF loading on output pins at 10% and 90% of V_{VDD}. Assumed transition timing on input pins is 5.5 ns.
3. t_{SYSCLK} is one period of the selected SYSCLK.

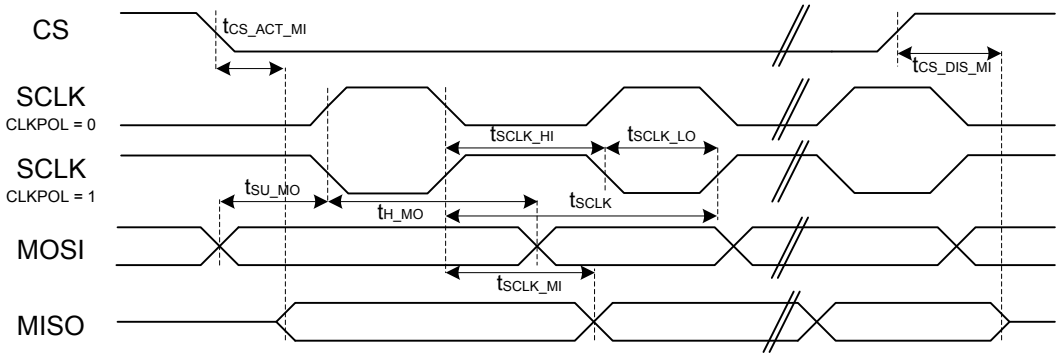

Figure 2.3. SPI Secondary Timing

2.2 Typical Performance Curves

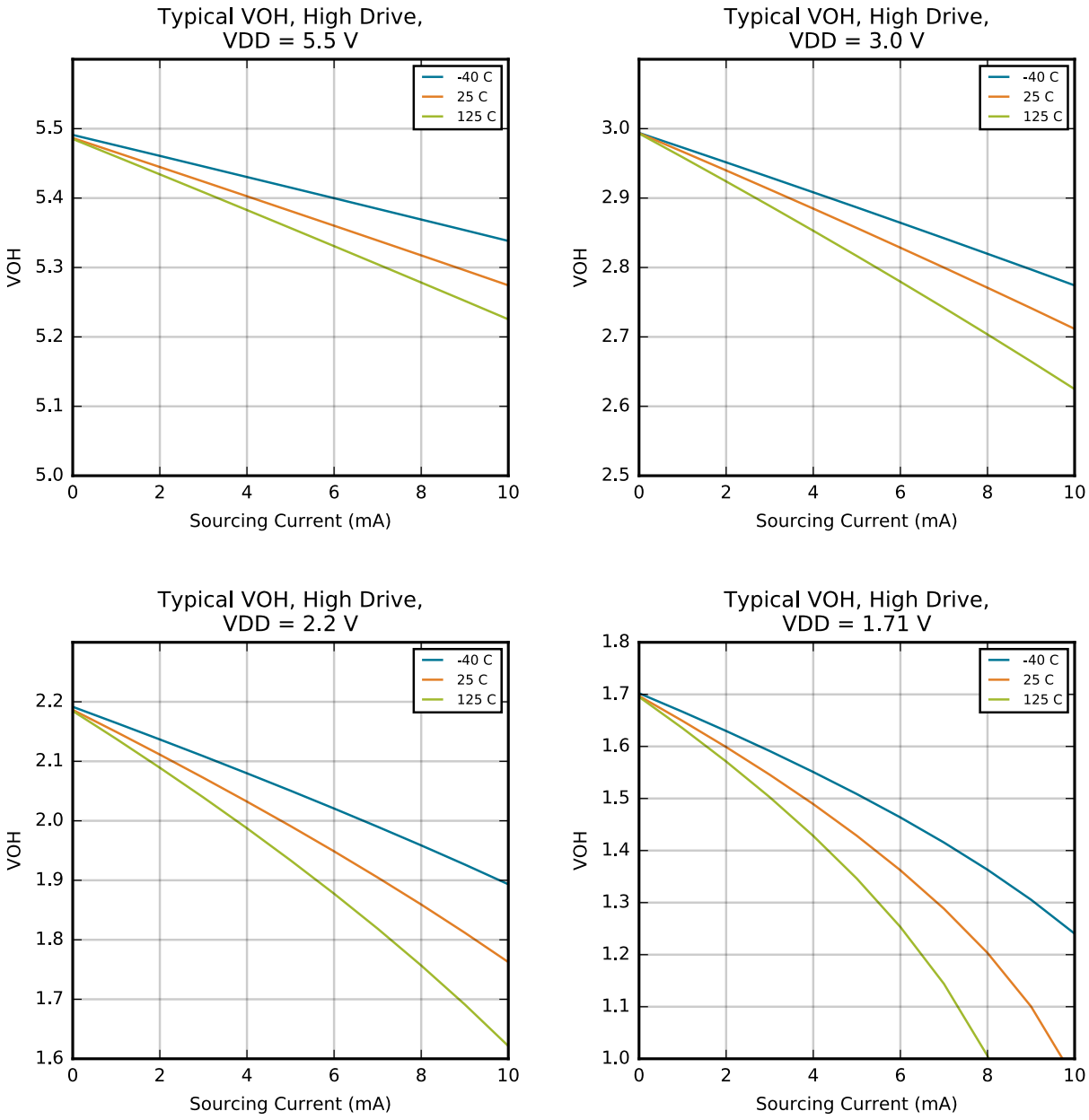

Figure 2.4. Typical V_{OH} vs. Load, High Drive

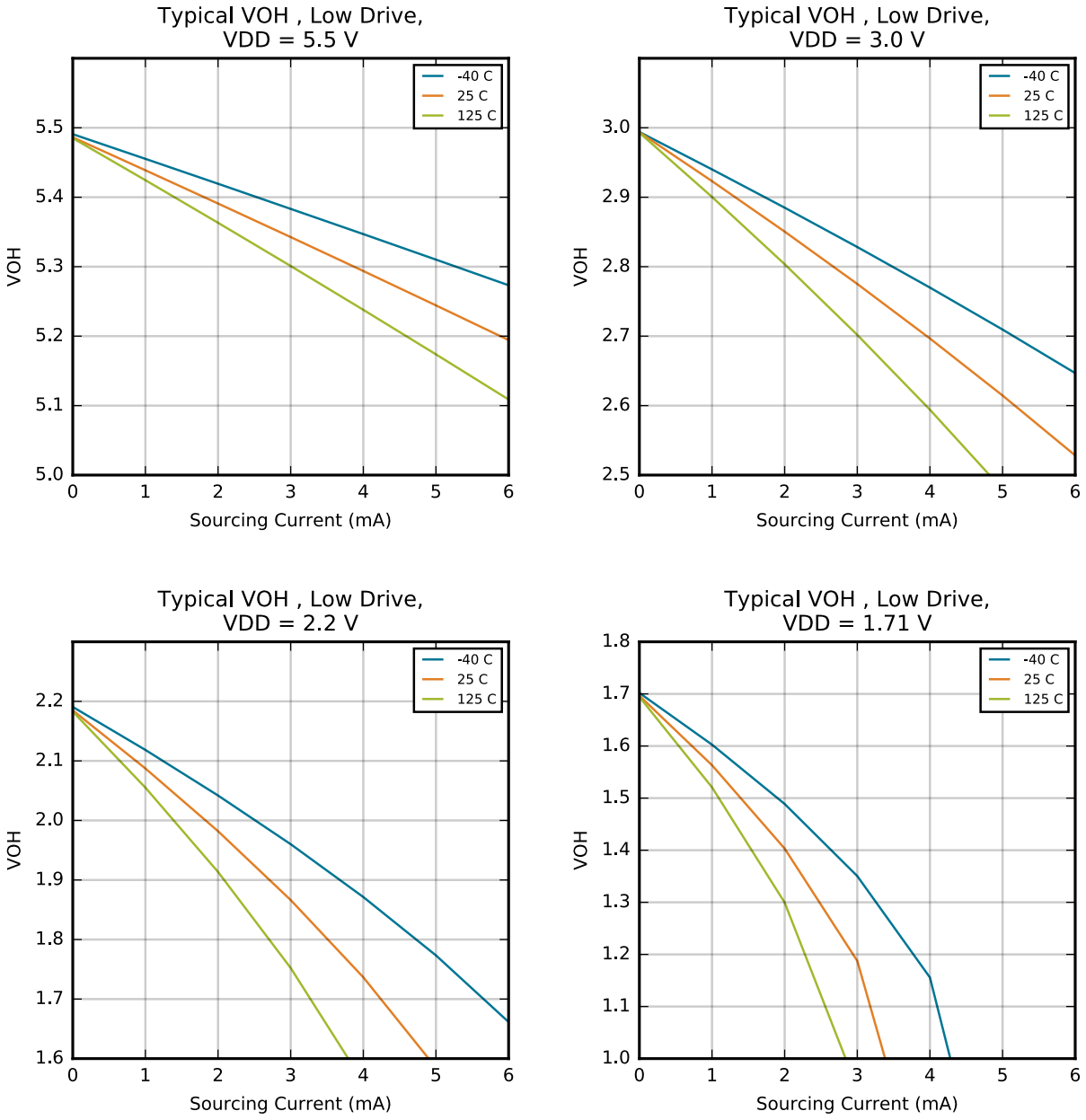

Figure 2.5. Typical V_{OH} vs. Load, Low Drive

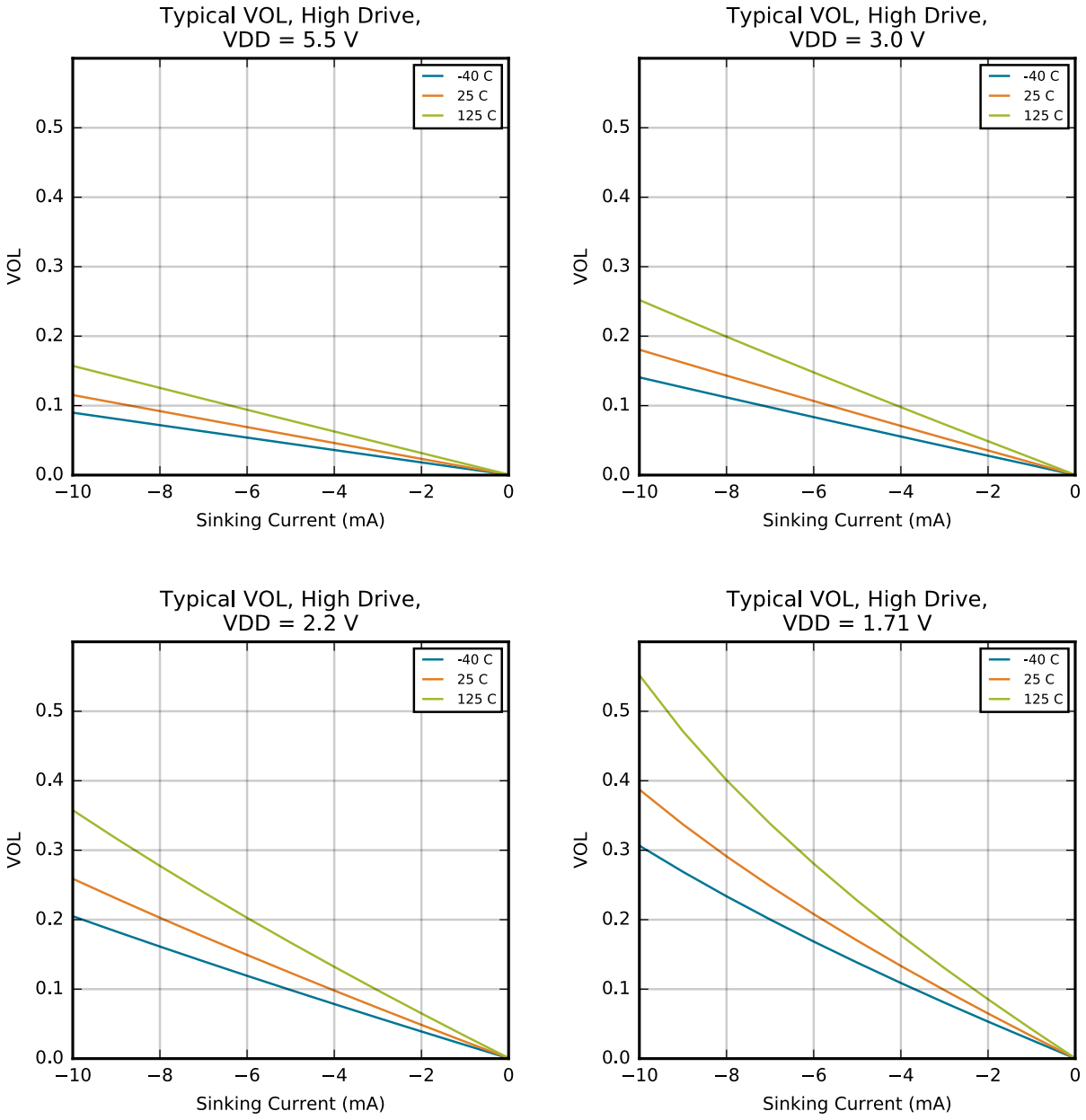

Figure 2.6. Typical V_{OL} vs. Load, High Drive

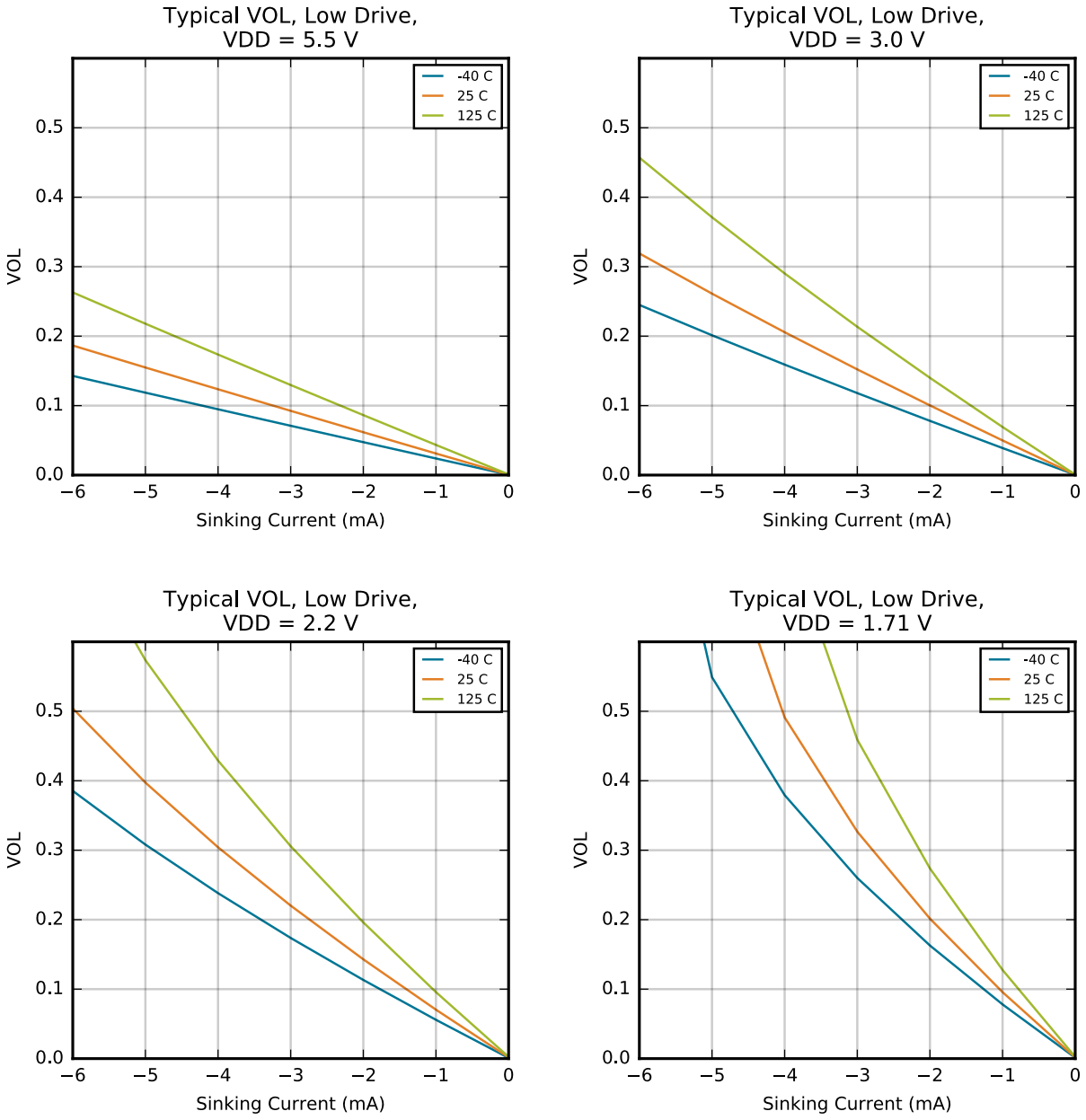

Figure 2.7. Typical V_{OL} vs. Load, Low Drive

3. Typical Connection Diagrams

3.1 Power

Figure 3.1 shows a typical connection diagram for the power pins of the EFM8BB52 devices.

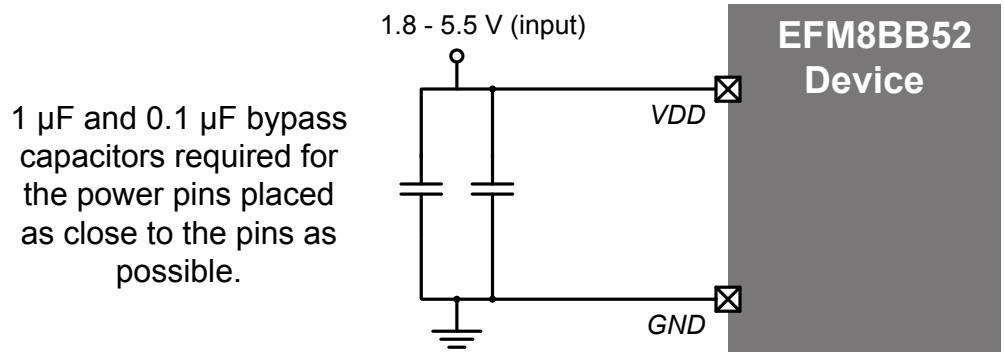

Figure 3.1. Power Connection Diagram

4. Pin Definitions

4.1 EFM8BB52-QFN32 Pin Definitions

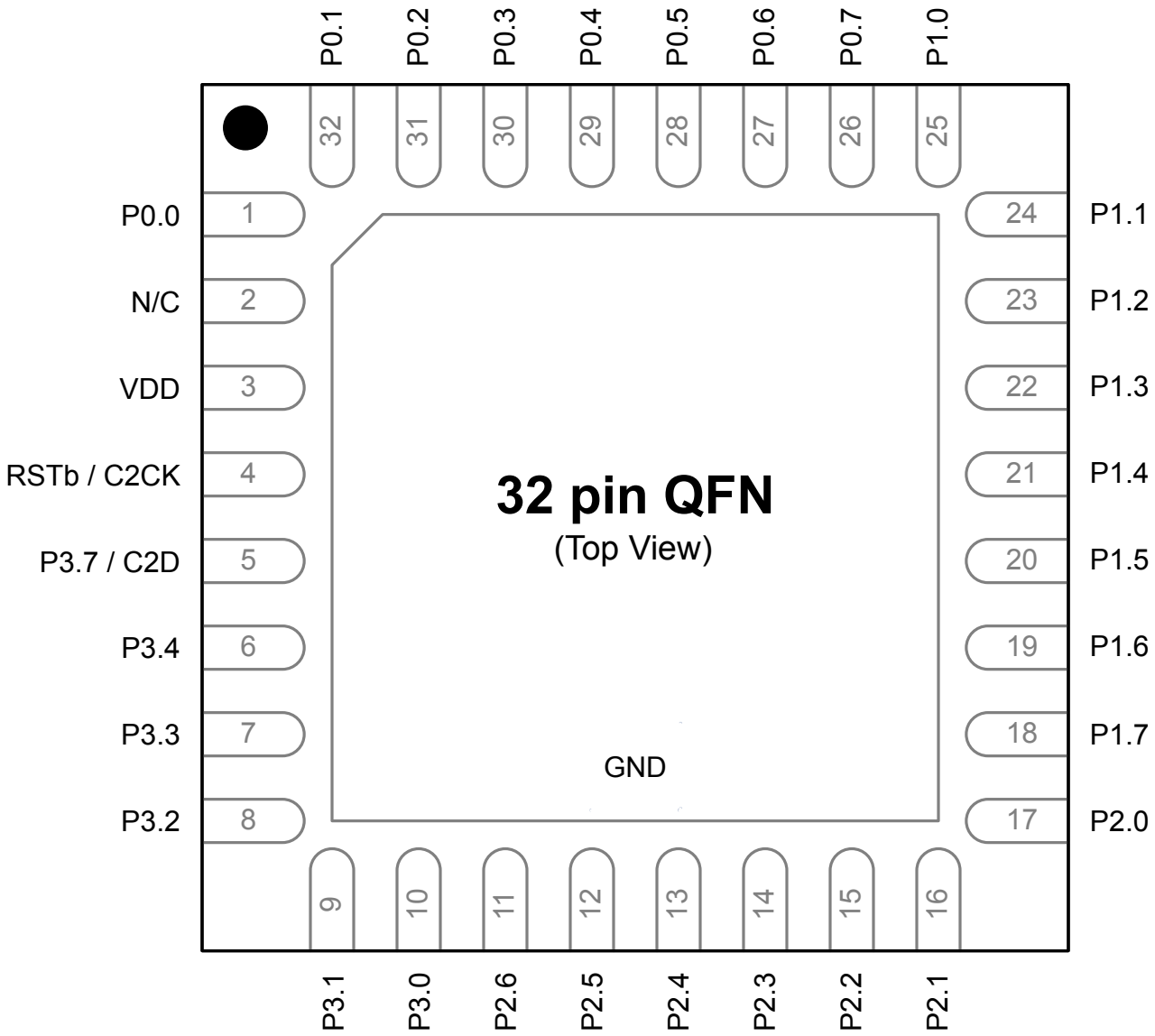

Figure 4.1. EFM8BB52-QFN32 Pinout

Table 4.1. Pin Definitions for EFM8BB52-QFN32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	ADC0.VREF CMP0.N0 DAC0.VREF VREFP.OUT
2	N/C	No Connect			
3	VDD	Supply Power Input			
4	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
5	P3.7 / C2D	Multifunction I/O / C2 Debug Data			
6	P3.4	Multifunction I/O			
7	P3.3	Multifunction I/O			
8	P3.2	Multifunction I/O			
9	P3.1	Multifunction I/O			CMP1.P10
10	P3.0	Multifunction I/O			ADC0.CH15 CMP1.N2 DAC0.OUT
11	P2.6	Multifunction I/O			CMP1.P9
12	P2.5	Multifunction I/O		CLU3.OUT	ADC0.CH14 CMP1.P8
13	P2.4	Multifunction I/O			ADC0.CH13 CMP1.P7
14	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	ADC0.CH12 CMP1.P6
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2.OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.CH11 CMP1.P5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
16	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	CMP1.P4
17	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	ADC0.CH10 CMP1.N1
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.CH9 CMP1.P3
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.CH8 CMP1.P2
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.CH7 CMP1.N0
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	CMP1.P1
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.CH6 CMP1.P0
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.CH5 CMP0.N2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	CMP0.P7
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1.OUT CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.CH4 CMP0.P6
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	CMP0.P5
27	P0.6	Multifunction I/O	Yes	P0MAT.6 INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	CMP0.P4
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.CH3 CMP0.N1

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.CH2 CMP0.P3
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	ADC0.CH1 CMP0.P2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0.OUT CLU0A.9 CLU2B.8 CLU3A.8	ADC0.CH0 CMP0.P1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.AGND CMP0.P0
Center	GND	Ground			

4.2 Crossbar Functional Map

The figure below shows all of the potential peripheral-to-pin assignments available to the crossbar. Note that this does not mean any peripheral can always be assigned to the highlighted pins. The actual pin assignments are determined by the priority of the enabled peripherals.

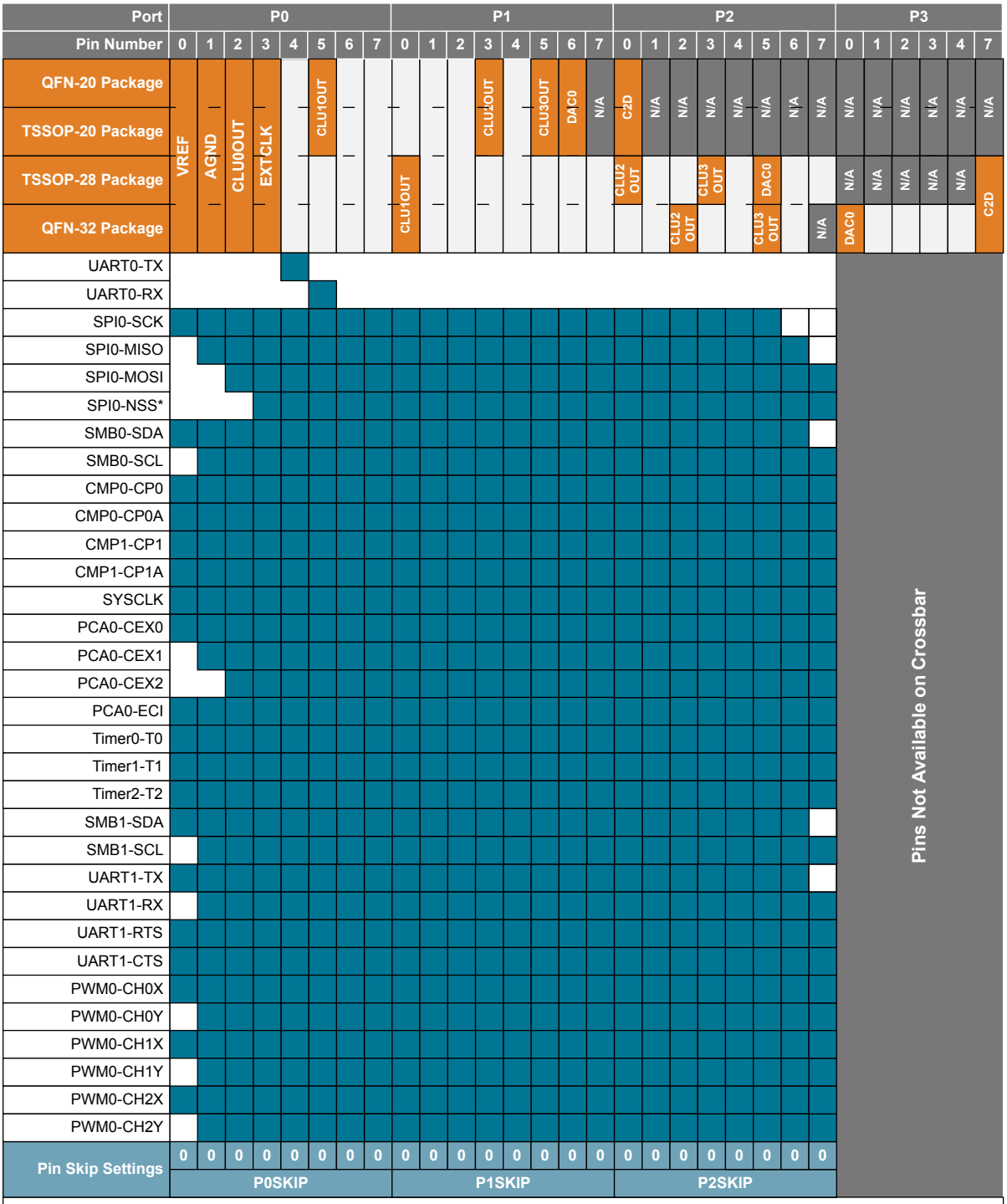

Figure 4.2. Full Crossbar Map

5. QFN32 Package Specifications

5.1 Package Dimensions

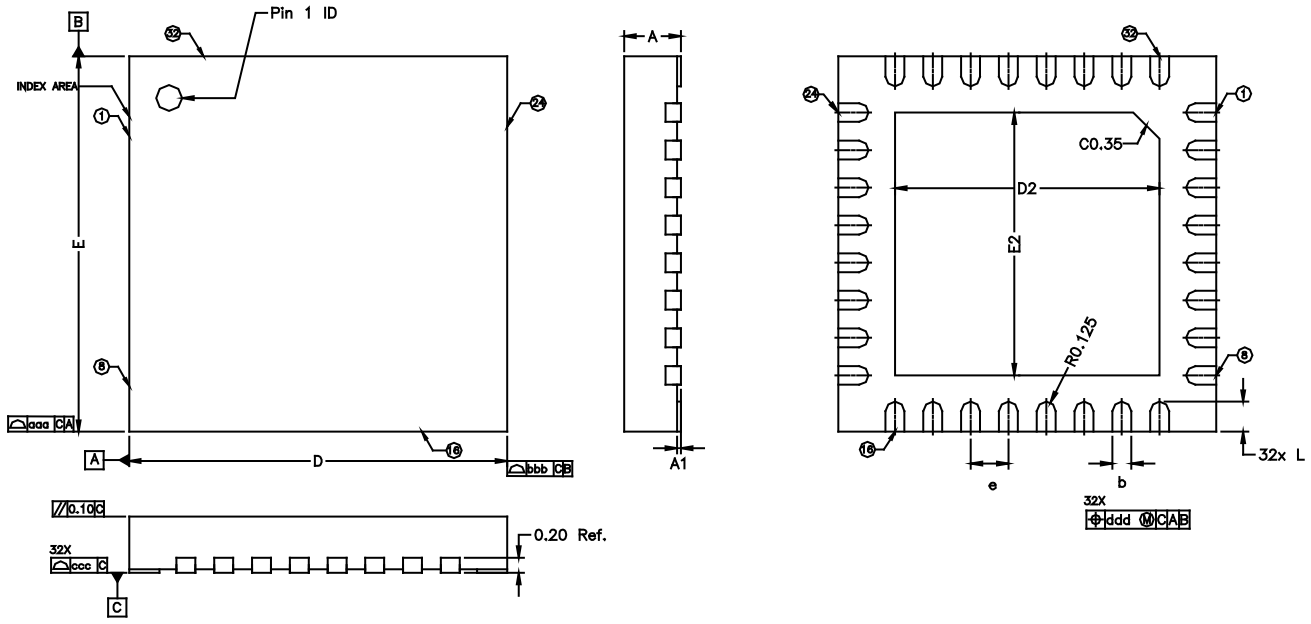

Figure 5.1. Package Drawing

Table 5.1. Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
D		5.00 BSC	
D2	3.40	3.50	3.60
e		0.50 BSC	
E		5.00 BSC	
E2	3.40	3.50	3.60
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	

Dimension	Min	Typ	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5.2 PCB Land Pattern

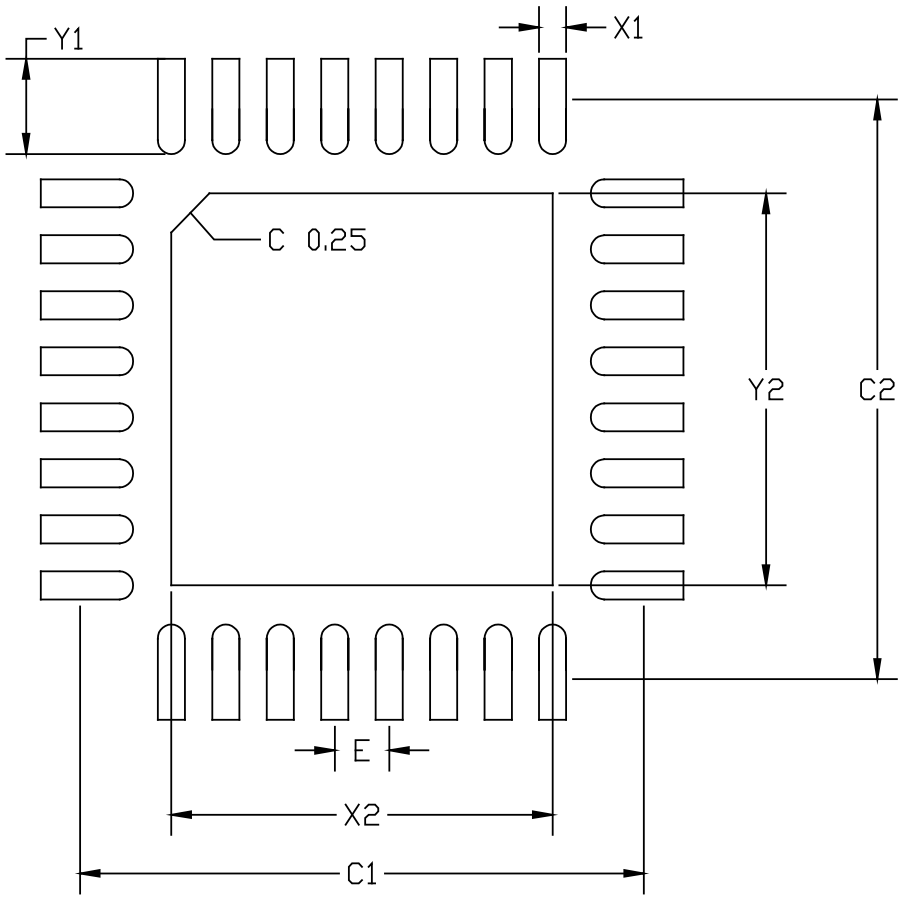

Figure 5.2. PCB Land Pattern Drawing

Table 5.2. PCB Land Pattern Dimensions

Dimension	mm
C1	4.90
C2	4.90
E	0.50
X1	0.30
Y1	0.85
X2	3.60
Y2	3.60

Dimension	mm

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 0.9 mm square openings on 1.2 mm pitch should be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5.3 Package Marking

Figure 5.3. Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

6. Revision History

Revision 1.0

September, 2021

Revision 0.1

November, 2020

- Initial release.